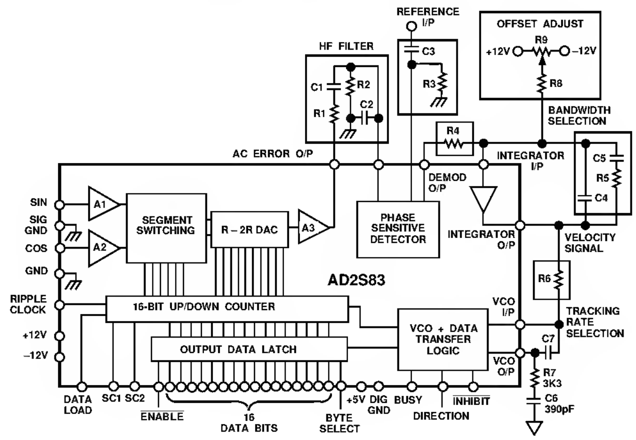
Variable Resolution, Resolver-to-Digital Converter

AD2S83

FEATURES
Tracking R/D Converter
High Accuracy Velocity Output
High Max Tracking Rate 1040 RPS (10 Bits)
10-, 12-, 14- or 16-Bit Resolution Set by User
Ratiometric Conversion
Stabilized Velocity Reference
Dynamic Performance Set by User
Industrial Temperature Range

APPLICATIONS
DC and AC Servo Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION
The AD2S83 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter.

The converter allows users to select their own resolution and dynamic performance with external components. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S83 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long leads allowing the converter to be located remote from the resolver.

The position output from the converter is presented via 3-state output pins which can be configured for operations with 8- or 16-bit bus. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data bus, and outputs are provided to allow for cycle or pitch counting in external counters.

A precise analog signal proportional to velocity is also available and will replace a tachogenerator.

The AD2S83 operates over reference frequencies in the range 0 Hz to 20,000 Hz.

PRODUCT HIGHLIGHTS
High Accuracy Velocity Output. A precision analog velocity signal with a typical linearity of ±0.1% and reversion error less than ±0.3% is generated by the AD2S83. The provision of this signal removes the need for mechanical tachogenerators used in servo systems to provide loop stabilization and speed control.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S83 to be 10, 12, 14 or 16 bits allowing optimum resolution for each application.

Ratiometric Tracking Conversion. This technique provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The component values are easy to select using the free component selection software design aid.

MODELS AVAILABLE
Information on the models available is given in the section "Ordering Information."

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AD2S83–SPECIFICATIONS ($\pm V_S = \pm 12$ V dc ± 5%; $V_L = +5$ V dc ± 10%; $T_A = -40°C$ to +85°C)

Parameter	Conditions	AD2S83A Min	Typ	Max	Units
SIGNAL INPUTS (SIN, COS)					
Frequency[1]		0		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
REFERENCE INPUT (REF)					
Frequency		0		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
PERFORMANCE					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	Degree
Max Tracking Rate	10 Bits	1040			rps
	12 Bits	260			rps
	14 Bits	65			rps
	16 Bits	16.25			rps
Bandwidth	User Selectable				
ACCURACY					
Angular Accuracy	A			**±8 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A			**4**	Codes
VELOCITY SIGNAL					
Linearity[2, 3, 4]	VCO Rate 0 kHz–500 kHz		±0.15	**±0.25**	%
	VCO Rate 500 kHz–1000 kHz		±0.25	**±1.0**	%
Reversion Error			±0.5	**±1.0**	% Output
DC Zero Offset[5]			±3		mV
Gain Scaling Accuracy			±1.5	**±3**	% FSR
Output Voltage	1 mA Load	±8			V
Dynamic Ripple	Mean Value			1.0	% rms O/P
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				Bits
Output Format	Bidirectional Natural Binary				
Load				**3**	LSTTL
$\overline{\text{INHIBIT}}$[6]					
Sense	Logic LO to $\overline{\text{INHIBIT}}$				
Time to Stable Data		240	390	490	ns
$\overline{\text{ENABLE}}$[6]	Logic LO Enables Position Output				
	Logic HI Outputs in High				
$\overline{\text{ENABLE}}$[6]/Disable Time	Impedance State	35		110	ns
BYTE SELECT[6]					
Sense					
Logic HI	MS Byte DB1–DB8				
Logic LO	LS Byte DB1–DB8				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High via 100 kΩ to $+V_S$				
SC1 SC2					
0 0	10-Bit Resolution				
0 1	12-Bit Resolution				
1 0	14-Bit Resolution				
1 1	16-Bit Resolution				

Parameter	Conditions		AD2S83		Units
		Min	Typ	Max	
$\overline{\text{COMPLEMENT}}$	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO to Activate; No Connect for Normal Operation				
$\overline{\text{DATA}}$ $\overline{\text{LOAD}}$					
Sense	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[6, 7]					
Sense	Logic HI When Position O/P Changing				
Width		200		**350**	ns
Load	Use Additional Pull-Up (See Figure 2)			1	LSTTL
DIRECTION[6]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				**3**	LSTTL
RIPPLE CLOCK[6]					
Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	**300**			ns
Reset	Before Next Busy				
Load				**3**	LSTTL
DIGITAL INPUTS					
Input High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 11.4$ V, $V_L = 5.0$ V	**2.0**			V
Input Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.0$ V			**0.8**	V
DIGITAL INPUTS					
Input High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			**±100**	µA
Input Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			**±100**	µA
DIGITAL INPUT					
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA}}$ $\overline{\text{LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**1.0**	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA}}$ $\overline{\text{LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**–400**	µA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	**2.4**			V
Low Voltage, V_{OL}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			**0.4**	V

NOTES
[1]Angular accuracy is not guaranteed <50 Hz reference frequency.
[2]Linearity derates from 500 kHz–1000 kHz @ 0.0017%/kHz.
[3]Refer to Definition of Linearity, "The AD2S83 as a Silicon Tachogenerator."
[4]Worst case reversion error at temperature extremes.
[5]Velocity output offset dependent on value for R6.
[6]Refer to timing diagram.
[7]Busy pulse guaranteed up to a VCO rate of 900 kHz.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

AD2S83–SPECIFICATIONS ($\pm V_S = \pm 12$ V dc ± 5%; $V_L = +5$ V dc ± 10%; $T_A = -40°C$ to +85°C)

Parameter	Conditions	AD2S83 Min	Typ	Max	Units
THREE-STATE LEAKAGE	DB1–DB16 Only				
Current I_L	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			**±20**	µA
	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			**±20**	µA
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Gain					
In Phase	w.r.t. REF	–0.882	–0.9	–0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	**150**	nA
Input Impedance		1.0			MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57	60	63	dB
Dead Zone Current (Hysteresis)		**90**	100	**110**	nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	**150**	nA
Output Voltage Range		**±8**			V
VCO					
Maximum Rate		1.1			MHz
VCO Rate	+ve DIR	**8.25**	8.50	**8.75**	kHz/µA
	–ve DIR	**8.25**	8.50	**8.75**	kHz/µA
VCO Power Supply Sensitivity					
Rate	$+V_S$			+0.5	%/V
	$-V_S$			–0.5	%/V
Input Offset Voltage			3		mV
Input Bias Current			12	**50**	nA
Input Bias Current Tempco			+0.22		nA/°C
Linearity of Absolute Rate					
0 kHz–500 kHz			±0.1	**±0.15**	%
500 kHz–1000 kHz			±0.15	**±1.0**	%
Reversion Error			±0.3	**±0.5**	% Output
POWER SUPPLIES					
Voltage Levels					
$+V_S$		+11.4		+12.6	V
$-V_S$		–11.4		–12.6	V
$+V_L$		+4.5	+5	$+V_S$	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	**±23**	mA
$\pm I_S$	$\pm V_S$ @ ±12.6 V		±19	**±30**	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	**±1.5**	mA

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specification subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Option*
AD2S83AP	–40°C to +85°C	8 arc min	P-44A

*P = Plastic Leaded Chip Carrier.

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2]	+13 V dc
$-V_S$	–13 V dc
$+V_L$	$+V_S$
Reference	+13 V to $-V_S$
SIN	+13 V to $-V_S$
COS	+13 V to $-V_S$
Any Logical Input	–0.4 V dc to $+V_L$ dc
Demodulator Input	+13 V to $-V_S$
Integrator Input	+13 V to $-V_S$
VCO Input	+13 V to $-V_S$
Power Dissipation	800 mW
Operating Temperature	
Industrial (AP)	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

CAUTION:

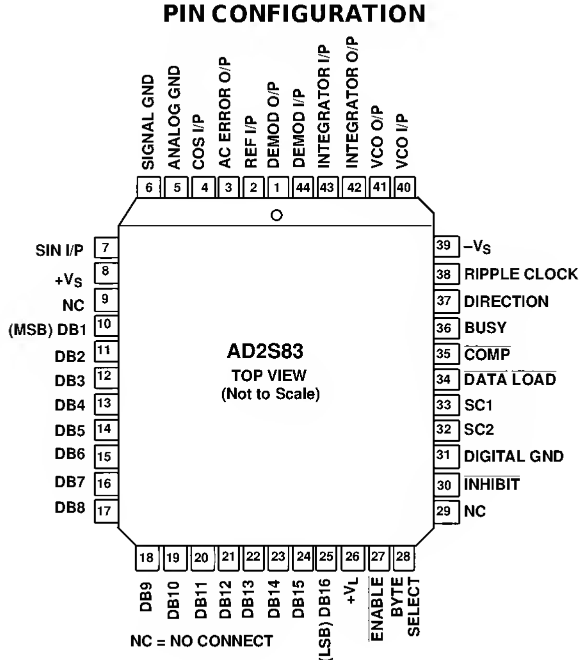
[1]Absolute Maximum Ratings are those values beyond which damage to the device may occur.

[2]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$)	±12 V dc ± 5%
Power Supply Voltage V_L	+5 V dc ± 10%
Analog Input Voltage (SIN and COS)	2 V rms ± 10%
Analog Input Voltage (REF)	1 V to 8 V peak
Signal and Reference Harmonic Distortion	10% (max)
Phase Shift Between Signal and Reference	±10 Degrees (max)
Ambient Operating Temperature Range	
Industrial (AP)	–40°C to +85°C

PIN CONFIGURATION



PIN DESIGNATIONS

Pin Nos.	Mnemonic	Description
1	DEMOD O/P	Demodulator Output
2	REFERENCE I/P	Reference Signal Input
3	AC ERROR O/P	Ratio Multiplier Output
4	COS	Cosine Input
5	ANALOG GND	Power Ground
6	SIGNAL GND	Resolver Signal Ground
7	SIN	Sine Input
8	$+V_S$	Positive Power Supply
10–25	DB1–DB16	Parallel Output Data
26	$+V_L$	Logic Power Supply
27	$\overline{\text{ENABLE}}$	Logic HI—Output Data Pins in High Impedance State Logic LO—Presents Active Data to the Output Pins
28	BYTE SELECT	Logic HI—Most Significant Byte to DB1–DB8 Logic LO—Least Significant Byte to DB1–DB8
30	$\overline{\text{INHIBIT}}$	Logic LO Inhibits Data Transfer to Output Latches
31	DIGITAL GND	Digital Ground
32, 33	SC2–SC1	Select Converter Resolution
34	$\overline{\text{DATA}}$ $\overline{\text{LOAD}}$	Logic LO DB1–DB16 Inputs Logic HI DB1–DB16 Outputs
35	$\overline{\text{COMPLEMENT}}$	Active Logic LO
36	BUSY	Converter Busy, Data not Valid While Busy HI
37	DIRECTION	Logic State Defines Direction of Input Signal Rotation
38	RIPPLE CLOCK	Positive Pulse When Converter Output Changes from 1s to All 0s or Vice Versa
39	$-V_S$	Negative Power Supply
40	VCO I/P	VCO Input
41	VCO O/P	VCO Output
42	INTEGRATOR O/P	Integrator Output
43	INTEGRATOR I/P	Integrator Input
44	DEMOD I/P	Demodulator Input

ESD SENSITIVITY

The AD2S83 features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharge (Human Body Model) and fast, low energy pulses (Charges Device Model).

Proper ESD protection are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices ESD Prevention Manual.

Bit Weight Table

Binary Bits (N)	Resolution (N^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and –12 V dc and must not be reversed. The voltage applied to V_L can be +5 V dc to $+V_S$.

It is recommended that the decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 µF (tantalum). Also capacitors of 100 nF and 10 µF should be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 10 and described in section "CONNECTING THE RESOLVER."

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally and as close to the converter as possible.

The external components required should be connected as shown in Figure 1.

CONVERTER RESOLUTION

Two major areas of the AD2S83 specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits; and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section COMPONENT SELECTION). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do it when the BUSY is low, i.e., when data is not changing.

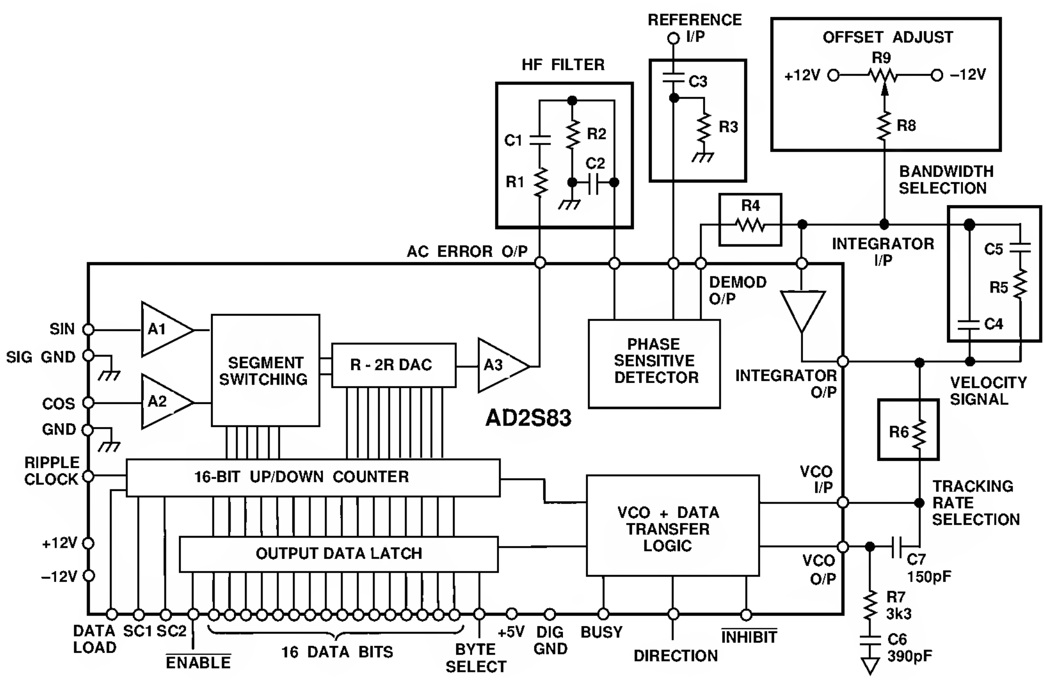


Figure 1. Connection Diagram

CONVERTER OPERATION

When connected in a circuit such as shown in Figure 10, the AD2S83 operates as a tracking resolver-to-digital converter. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S83 is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures high immunity to signals that are not phase or frequency coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING

The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S83 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S83 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak.) Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word. As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the inverse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changing state (1 LSB min change in input) with a corresponding change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$. The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR INPUT (which can be trimmed out—see Figure 1), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S83 can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL

The tracking converter technique generates an internal signal at the output of the integrator (INTEGRATOR OUTPUT) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

It is recommended that the velocity output be buffered.

The sense is positive for an increasing angular input and negative for decreasing angular input. The full-scale velocity output is ±8 V dc. The output velocity scaling and tracking rate are a function of the resolution of the converter; this is summarized below.

Res	Max Tracking Rate (rps)	Nominal Scaling (rps/V dc)
10	1040	130
12	260	32.5
14	65	8.125
16	16.25	2.03

(Velocity O/P = ±8 V dc nominal)

The output velocity can be suitably scaled and used to replace a conventional DC tachogenerator. For more detailed information see "AD2S83 as a Silicon Tachogenerator" section.

DC ERROR SIGNAL

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. As the converter is a Type 2 servo loop, the demodulator output signal will increase if the output fails to track the input for any reason. This is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal or external malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in-test."

COMPONENT SELECTION

The following instructions describe how to select the external components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used, and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

Free *PC compatible software is available to help users select the optimum component values for the AD2S83, and display the transfer gain, phase and small step response.*

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S83, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted—in which case R2 = R3 and C1 = C3, calculated below—but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.

   Values should be chosen so that

$$15\,k\Omega \leq R1 = R2 \leq 56\,k\Omega$$

$$C1 = C2 = \frac{1}{2\pi R1\, f_{REF}}$$

   and f_{REF} = Reference Frequency (Hz)

   This filter gives an attenuation of three times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4) (See Phase Sensitive Demodulator Section)
   If R1, C2 are fitted then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\,\Omega$$

   where 100×10^{-9} = current/LSB
   If R1, C2 are not fitted then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\,\Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling of the DC ERROR in volts/LSB

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100\,k\Omega$$

$$C3 > \frac{1}{R3 \times f_{REF}}\,F$$

   with R3 in Ω.

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate, the velocity output will be 8 V.

   Decide on your maximum tracking rate, "T," in revolutions per second. When setting the value for R6, it should be remembered that the linearity of the velocity output is specified across 0 kHz–500 kHz and 500 kHz–1000 kHz. The following conversion can be used to determine the corresponding rps:

$$rps = \frac{VCO\ Rate(Hz)}{2^{N}}$$

   Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{6.81 \times 10^{10}}{T \times n}\,\Omega$$

   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does not exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100 Hz for a 400 Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.

   b. Select C4 so that

$$C4 = \frac{21}{R6 \times f_{BW}^{\,2}}\,F$$

   with R6 in Ω and f_{BW}, in Hz selected above.

   c. C5 is given by

$$C5 = 5 \times C4$$

   d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\,\Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be connected as close as possible to the VCO output, Pin 41.

$$C6 = 390\ pF,\ R7 = 3.3\,k\Omega$$

7. VCO Optimization
   To optimize the performance of the VCO a capacitor, C7, should be placed across the VCO input and output, Pins 40 and 41.

$$C7 = 150\ pF$$

8. Offset Adjust

Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

If fitted, the following values of R8 and R9 should be used:

$$R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega \text{ potentiometer}$$

To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 490 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL level. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input selects the byte of the position data to be presented at the data output DB1 to DB8. The least significant byte will be presented on data output DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S83 is used with a resolution less than 16 bits the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output DB1 and DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK

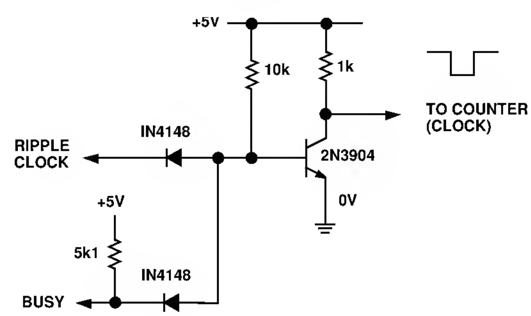
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulse width of the ripple clock is 300 ns. RIPPLE CLOCK is normally set high before a BUSY pulse and resets before the next positive going edge of the next BUSY pulse.

The only exception to this is when DIR changes while the RIPPLE CLOCK is high. Resetting of the RIPPLE clock will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

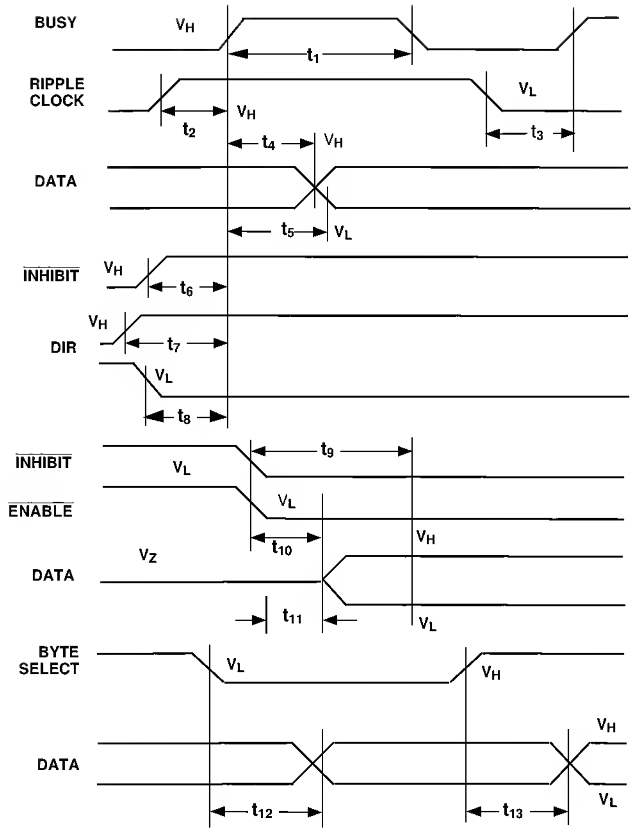
If the AD2S83 is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2).

RIPPLE CLOCK is unaffected by $\overline{\text{INHIBIT}}$.



NOTE: DO NOT USE ABOVE CCT WHEN $\overline{\text{INHIBIT}}$ IS LOW.

Figure 2. Diode Transistor Logic Nand Gate



Digital Timing

Parameter	T_{MIN}*	T_{MAX}*	Condition
t_1	200	350	BUSY WIDTH V_H-V_H
t_2	10	25	RIPPLE CLOCK V_H to BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L to Next BUSY V_H
t_4	16	45	BUSY V_H to DATA V_H
t_5	3	25	BUSY V_H to DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H to BUSY V_H
t_7	485	625	MIN DIR V_H to BUSY V_H
t_8	515	670	MIN DIR V_H to BUSY V_H
t_9	–	490	$\overline{\text{INHIBIT}}$ V_L to DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L to DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L to DATA V_L
t_{12}	60	140	BYTE SELECT V_L to DATA STABLE
t_{13}	60	125	BYTE SELECT V_H to DATA STABLE

*ns

DIRECTION Output

The DIRECTION (DIR) output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA and RIPPLE CLOCK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This occurs when the direction of rotation of the input changes but the magnitude of the rotation is less than 1 LSB.

$\overline{\text{COMPLEMENT}}$

The $\overline{\text{COMPLEMENT}}$ input is an active low input and is internally pulled to $+V_S$ via 100 kΩ.

Strobing $\overline{\text{DATA LOAD}}$ and $\overline{\text{COMPLEMENT}}$ pins to logic LO will set the logic HI bits of the AD2S83 counter to a LO state. Those bits of the applied data which are logic LO will not change the corresponding bits in the AD2S83 counter.

For Example:

Initial Counter State	10101
Applied Data Word	11000
Counter State after $\overline{\text{DATA LOAD}}$	11000
Initial Counter State	10101
Applied Data Word	11000
Counter State after $\overline{\text{DATA LOAD}}$ and Complement	00101

In order to read the counter following a $\overline{\text{DATA LOAD}}$, the procedure below should be followed:

1. Place outputs in high impedance state ($\overline{\text{ENABLE}}$ = HI).
2. Present data to pins.
3. Pull $\overline{\text{DATA LOAD}}$ and $\overline{\text{COMPLEMENT}}$ pins to ground.
4. Wait 100 ns.
5. Remove data from pins.
6. Remove outputs from high impedance state ($\overline{\text{ENABLE}}$ = LO).
7. Read outputs.

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The AD2S83 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1. The section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the AD2S83 and the variations in the dynamic performance available to the user.

Loop Compensation

The AD2S83 (connected as shown in Figure 1) operates as a Type 2 tracking servo loop where the VCO/counter combination and Integrator perform the two integration functions inherent in a Type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize the loop.

This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response the converter is that of a unity gain second order low-pass filter, with the angle of the resolver as the input and the digital position data as the output.

The AD2S83 does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer. (For more information contact Motion Control Applications.)

A block diagram of the AD2S83 is given in Figure 3.

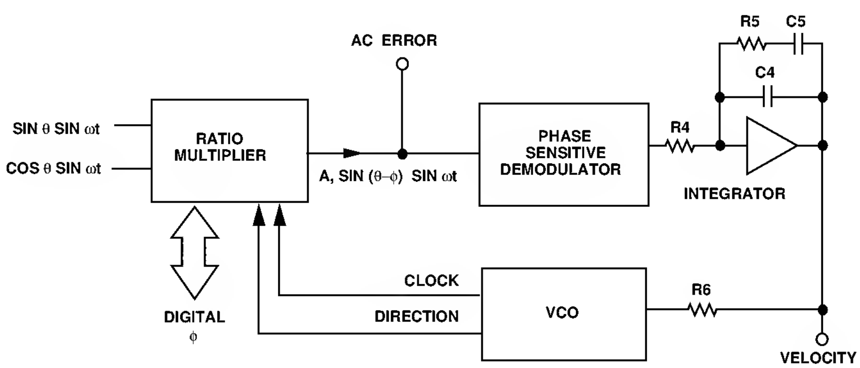


Figure 3. Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the AD2S83. This compares the signal from the resolver (angle θ) to the digital (angle ϕ) held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by an electromechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin \omega t$$

where $\omega = 2 \pi f_{REF}$

f_{REF} = reference frequency

A1 = the gain of the ratio multiplier stage = 14.5.

So for 2 V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{n}\right) \times A1$$

where n = bits per rev
= 1,024 for 10-bit resolution
= 4,096 for 12-bit resolution
= 16,384 for 14-bit resolution
= 65,536 for 16-bit resolution

giving an AC ERROR output
= 178 mV/bit @ 10-bit resolution
= 44.5 mV/bit @ 12-bit resolution
= 11.125 mV/bit @ 14-bit resolution
= 2.78 mV/bit @ 16-bit resolution

The ratio multiplier will work in exactly the same way whether the AD2S83 is connected as a tracking converter or as a control transformer, where data is preset into the counters using the $\overline{\text{DATA}}$ $\overline{\text{LOAD}}$ pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the AD2S83 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of three times at the input to the phase sensitive demodulator.

Values of components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (\text{DEMODULATOR INPUT rms voltage})$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160 mV/bit (10-bit resolution)
= 40 mV/bit (12-bit resolution)
= 10 mV/bit (14-bit resolution)
= 2.5 mV/bit (16-bit resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the AD2S83 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 LSB. In order to ensure that this feedback "hysteresis" is set to 1 LSB the input current to the integrator must be scaled to be 100 nA/bit. Therefore,

$$R4 = \frac{\text{DC Error Scaling (mV/bit)}}{100\ (\text{nA/bit})}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100 nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocking either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the VCO reset period the input continues to be integrated. The reset period is constant at 40 ns.

The VCO rate is fixed for a given input current by the VCO scaling factor:

$$= 8.5\ \text{kHz}/\mu\text{A}$$

The tracking rate in rps per µA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5 V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$$(100 \times 4096)/(8500) = 48.2\ \mu\text{A}$$

Thus, R6 would be set to: $5/(48.2 \times 10^{-6}) = 103.7\ \text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

$$\text{Velocity Offset Voltage} = \text{R6} \times (\text{VCO bias current})$$

The temperature coefficient of this offset is given by

$$\text{Velocity Offset Tempco} = \text{R6} \times (\text{VCO bias current tempco})$$

where the VCO bias current tempco is typically +0.22 nA/°C.

The maximum recommended rate for the VCO is 1.1 MHz which sets the maximum possible tracking rate.

Since the minimum voltage swing available at the integrator output is ±8 V, this implies that the minimum value for R6 is 62 kΩ. As

$$\text{Max Current} = \frac{1.1 \times 10^{6}}{8.5 \times 10^{3}} = 129\ \mu\text{A}$$

$$\text{Min Value R6} \frac{8}{129 \times 10^{-6}} = 62\ \text{k}\Omega$$

Transfer Function

By selecting components using the method outlined in the section "Component Selection," the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1 + s_N)}{(s_N + 2.4)(s_N^2 + 3.4\, s_N + 5.8)}$$

where, s_N, the normalized frequency variable is given by:

$$s_N = \frac{2}{\pi}\ \frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3 dB bandwidth (selected by the choice of external components).

The acceleration constant K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2\ \text{sec}^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

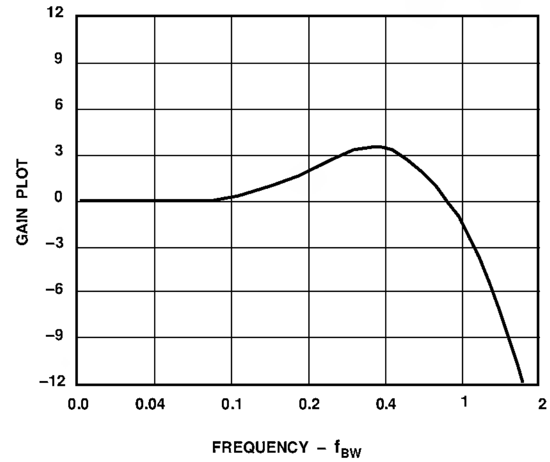


Figure 4. Gain Plot

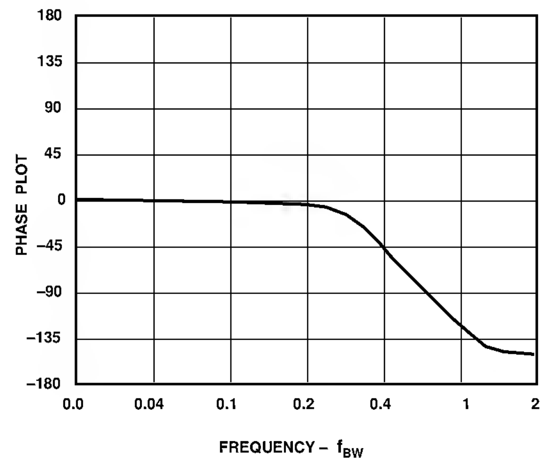


Figure 5. Phase Plot

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1, and the t_2 is the time from the step until the converter is settled to 1 LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

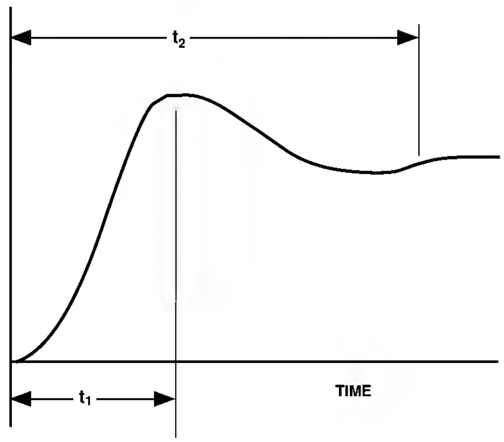


Figure 6. Small Step Response

The large signal step response (for steps greater than 5 degrees) applies when the error voltage exceeds the linear range of the converter.

Typically the converter will take three times longer to reach the first peak for a 179 degrees step.

In response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

THE AD2S83 AS A SILICON TACHOGENERATOR

Position Control Using the AD2S83

The AD2S83 has been optimized for use as a feedback device for velocity as well as position. A traditional position control loop shown below compares a demand position with an actual to derive a position error and hence a velocity demand.

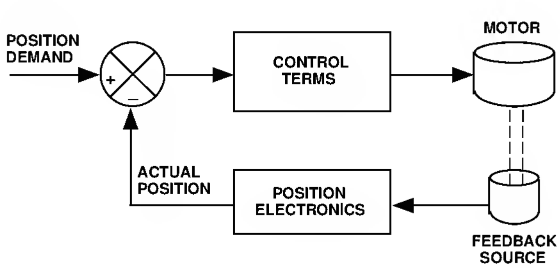


Figure 7. Position Control

Quality of control may be reduced if the load on a motor varies dynamically. System reaction and compensation for a sudden change in the loading depends on how rapidly the system can update the velocity demand to the motor. This can cause rapid acceleration of the motor until the loop updates with a new velocity demand.

The only effective way to compensate for dynamic loading effects is to introduce a 2nd order term which will provide the motor with an acceleration or deceleration demand signal (see Figure 8).

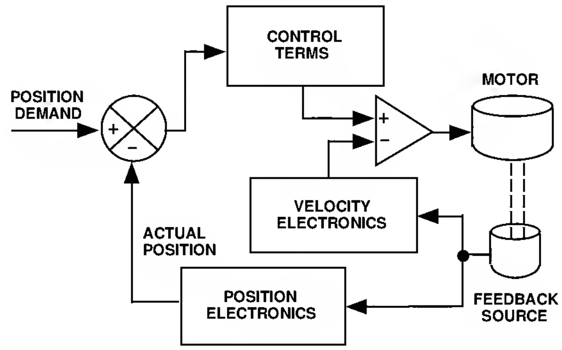


Figure 8. Position Control and Velocity Control

Traditionally this would need to be implemented by using separate position and speed feedback transducers, e.g., an encoder or resolver and a dc tachogenerator. The AD2S83 can decode the resolver to provide both velocity and position information.

DC Tachogenerator

The DC tachogenerator is a small permanent magnet dc generator. The output is a dc voltage which is proportional to the speed of the rotor and whose polarity is determined by the direction of rotation. Physically they are similar to a resolver.

Velocity Error Derivation

The velocity error is the difference between the synthesized dc velocity demand derived from the actual and demand positions and the feedback from the tachogenerator or the AD2S83. The velocity demand is usually derived via a DAC so apart from any quantization noise it is clean. The velocity feedback, therefore, needs to be as close to a pure dc level as possible. The errors which determine the quality of the resultant acceleration demand to the motor are explained below.

Linearity

Linearity is the maximum deviation from the ideal straight line velocity characteristic. The line used is given by:

$$v = mx + c$$

where v = velocity
m = gain scaling
x = dc voltage
c = zero velocity dc offset

Linearity is generally a function of the input velocity to the tachogenerator or resolver.

Reversion Error

Reversion or reversal error is an offset which is dependent on the direction of rotation of the transducer; e.g., if 10 rps = 1.000 V dc, then –10 rps = 1.003 V dc with +0.3% reversion error and FSO = ±8 V dc.

Zero Velocity DC Offset

This is a residual dc offset present at zero input velocity. This can be externally nulled.

Ripple Content

Ripple content is due to several factors. Tachogenerators suffer from ripple due to the speed of rotation, commutator segments and the number of poles. The resolver/RDC combination has a predominant ripple at twice the resolver reference as a result of the synchronous demodulator and at a frequency twice per revolution due to the resolver windings mismatch.

Motor torque pulsations which are a consequence of excessive velocity ripple have a detrimental effect upon the quality of speed control in servo systems.

The resultant "cogging" effect will be particularly noticeable at low speed and when the motor is in the low torque region.

Other undesirable side effects such as the increase in acoustic noise from a motor and a temperature rise in the motor stator windings are possible results of the presence of torque ripple.

For more detailed information of the causes and sources of errors see section "Velocity Errors."

AD2S83 COMPARISON WITH DC TACHOGENERATOR

Comparative tests of the AD2S83 and a dc tachogenerator were carried out. The tachogenerator was connected at the nondrive end of the motor shaft with the resolver located behind the drive shaft of the motor. The AD2S83 was located remotely. The AD2S83 was set up with a 200 Hz bandwidth, reference frequency of 2.6 kHz and resolution of 14 bits.

The comparative analysis can be summarized:

	AD2S83	DC Tacho	Conditions
Linearity %	0.1	0.1	0-3600 rpm
Reversion Error % FSO	0.3	0.25	

Note the typical operating range of dc tachogenerator is 0 rpm-3600 rpm. The resolver/AD2S83 combination will operate up to speeds in excess of 10000 rpm.

Ripple Effects

The comparative analysis of the output ripple from the tachogenerator and the AD2S83 is illustrated below.

Minimization of the AD2S83 output ripple is discussed in detail in section "Velocity Errors."

Other Factors

Other factors concerning choice of feedback source have to be addressed. On average the MTBF of a tachogenerator is 347 days as opposed to typically 8 years for a resolver. Resolvers are relatively insensitive to temperature whereas a tachogenerator will be specified up to a maximum of 100°C with a ±0.1%/°C (above 25°C) degradation in output voltage. The brushless resolver requires no preventative maintenance; the brushes on a tachogenerator, however, will require periodic checking.

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{\text{Input Acceleration}}{\text{Error in Output Angle}}$$

The numerator and denominator must have consistent angular units. For example if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error output in degrees.

K_A does not define maximum input acceleration, only the error due to acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$\text{Angular Accuracy} \times K_A = \text{Degrees/sec}^2$$

K_A can be used to predict the output position error for a given input acceleration. For example for an acceleration of 100 revs/sec^2, $K_A = 2.7 \times 10^6$ sec^{-2} and 12-bit resolution.

$$\text{Error in LSBs} = \frac{\text{Input acceleration } [LSB/sec^2]}{K_A [sec^{-2}]}$$

$$= \frac{100\,[rev/sec^2] \times 2^{12}}{2.7 \times 10^6} = 0.15 \text{ LSBs or } 47.5 \text{ seconds of arc}$$

To determine the value of K_A based on the passive components used to define the dynamics of the converter the following should be used.

$$K_A = \frac{4.04 \times 10^{11}}{2^n \times R6 \times R4 \times (C4 + C5)}$$

Where n = resolution of the converter.
R4, R6 in ohms
C5, C4 in farads.

SOURCES OF ERRORS

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator. This offset will be treated as an error signal. The resulting angular error will typically be 1 arc minute over the operating temperature range.

A description of how to adjust the zero offset is given in the section "COMPONENT SELECTION"; the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$\text{Error} = 0.53\ a \times b \text{ arc minutes}$$

where a = differential phase shift (degrees).
b = signal to reference phase shift (degrees).

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions the extra error can be made insignificant.

Most resolvers exhibit a phase shift between the signal and the reference. This phase shift will, however, give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (rps)} \times \text{Phase Shift (Degrees)}}{\text{Reference Frequency}} = \text{Error Degrees}$$

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5 kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \text{ Degrees}$$

This effect can be eliminated by placing a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY ERRORS

Some "ripple" or noise will always be present in the velocity signal. Velocity signal ripple is caused by, or related to, the following parameters. The resulting effects are generally additive. This means diagnosis needs to be an iterative process in order to define the source of the error.

1.0 Reference Frequency
A ripple content at the reference frequency is superimposed on the velocity signal output. The amplitude depends on the loop bandwidth. This error is a function of a dc offset at the input to Phase Sensitive Demodulator (PSD).

2.0 Resolver Inaccuracies
Impedance mismatch occur in the sine and cosine windings of the resolver. These give rise to differential phase shift between the sine and cosine inputs to the RDC and variations in the resolver output amplitudes.

2.1 Sine and Cosine Amplitude Mismatch
This is normally identified by the presence of asymmetrical ripple voltages.

2.2 Differential Phase Shift between the Sine and Cosine Inputs
The frequency of this ripple is usually twice the input velocity, and the amplitude is proportional to the magnitude of the velocity signal. The phase shift is normally induced through the connections from the resolver to the converter. Maintaining equal lengths of screened twisted pair cable from the resolver to the AD2S83 will reduce the effects of resistive imbalance, and therefore, reduce differential phase shift.

3.0 LSB Update Ripple
LSB update noise occurs as the resolver rotates and the digital outputs of the RDC are updated. For a correctly scaled loop, this ripple component has a magnitude of approximately 2 mV peak at 16-bit resolution.

3.1 Ripple due to the LSB rate given by:
LSB rate = N × Reference Frequency
The PSD generates sums and differences of all its component input frequencies, so when the LSB update rate is an multiple of the reference frequency, a beat frequency is generated. The magnitude of this ripple is a function of the LSB weighting, i.e., ripple is less at 16 bits.

4.0 Torque Ripple
Torque ripple is a phenomenon associated with motors. An ac motor naturally exhibits a sinusoidal back emf. In an ideal system the current fed to the motor should, in order to cancel, also be sinusoidal. In practice the current is often trapezoidal. Consequently, the output torque from the motor will not be smooth and torque ripple is created. If the loading on a motor is constant, the velocity of the motor shaft will vary as a result of the cyclic variation of motor torque. The variation in velocity then appears on the velocity output as ripple. This is not an error but a true velocity variation in the system.

Offset Errors

The limiting factor in the measuring of low or "creep" speeds is the level of dc offset present at zero velocity. The zero velocity dc offset at the output of the AD2S83 is a function of the input bias current to the VCO and the value for the input resistor R6. See "Circuit Functions and Dynamic Performance VCO."

The offset can be minimized by reducing the maximum tracking rate so reducing the value for R6. Offset is a function of tracking rate and therefore resolution; the dc offset is lowest at 16 bits. To increase the dynamic range of the velocity dynamic resolution switching can be employed. (Contact MCG Applications for more information.)

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 10.

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assume that R1 = R2 = R and C1 = C2 = C

and Reference Frequency = $\frac{1}{2\pi RC}$.

By altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

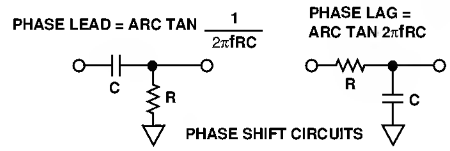


Figure 9. Phase Shift Circuits

TYPICAL CIRCUIT CONFIGURATION

Figure 10 shows a typical circuit configuration for the AD2S83 with 12-bit resolution. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 2.7×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

For more information on resistive scaling of SIN, COS and REFERENCE converter inputs refer to the application note, "Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters."

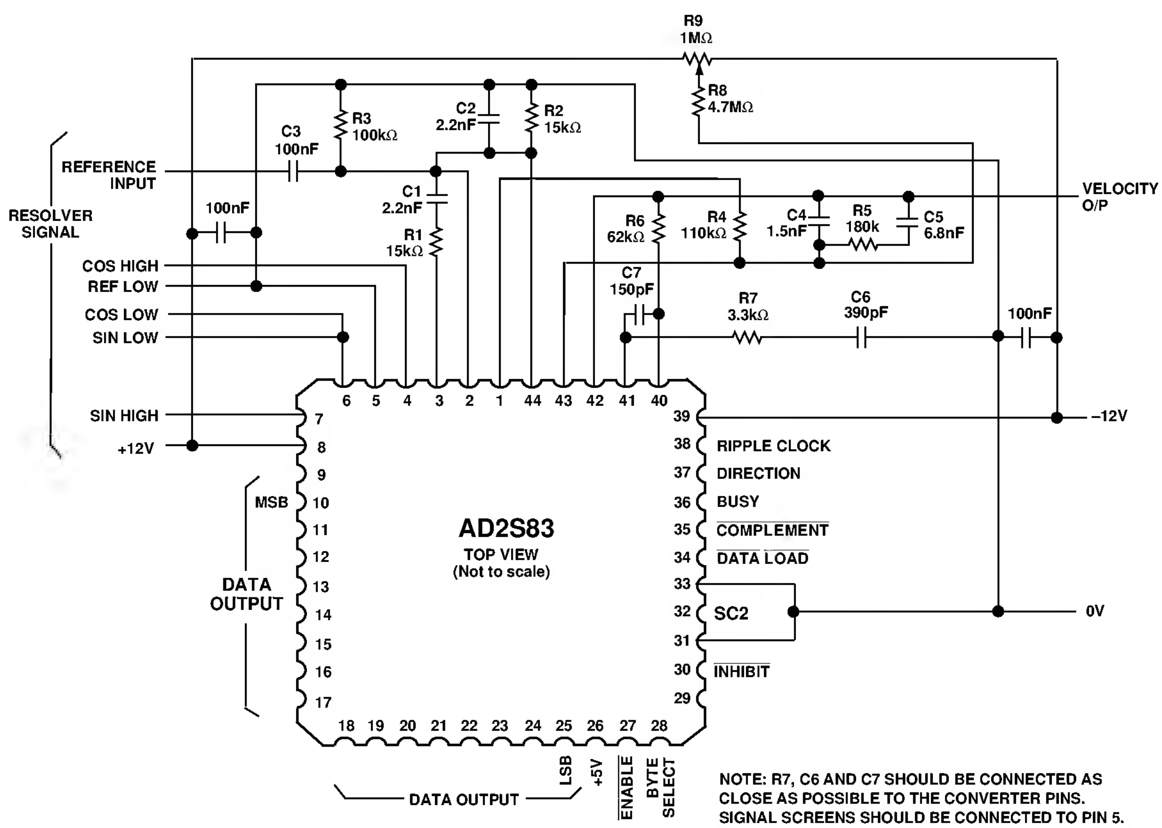


Figure 10. Typical Circuit Configuration

APPLICATIONS

Control Transformer

The ratio multiplier of the AD2S83 can be used independently of the loop integrators as a control transformer. In this mode, the resolver inputs θ are multiplied by a digital angle ϕ, any difference between ϕ and θ will be represented by the AC ERROR output as Sin ωt sin $(\theta-\phi)$ or the DEMOD output as sin $(\theta-\phi)$. To use the AD2S83 in this mode refer to the "Control Transformer" application note.

OTHER PRODUCT

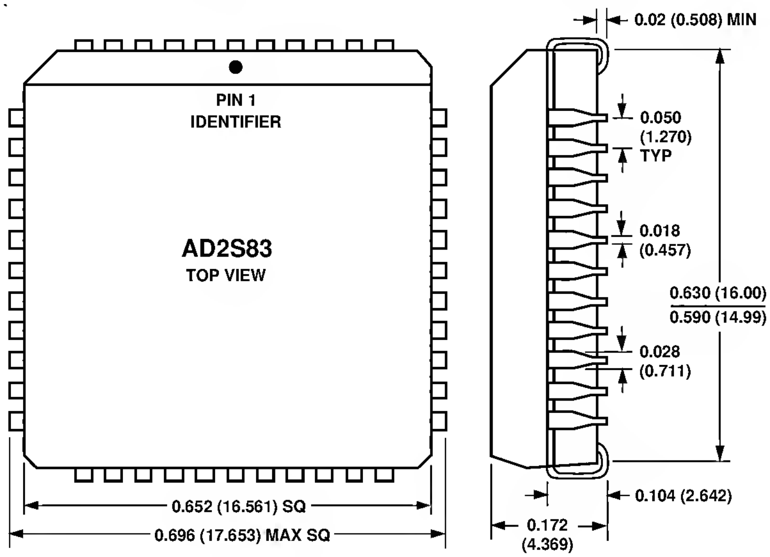
AD2S90. Low-cost resolver-to-digital converter with outputs which emulate optical encoders and a serial output for absolute position information. Unlike the AD2S83, the AD2S90 requires no external components to operate. The AD2S90 is built on LC^2MOS and packaged in a 20-pin PLCC.

AD2S80A/81A/82A. Monolithic resolver-to-digital converter. The AD2S80/82A offer selectable 10, 12, 14, 16 bits of resolution. The AD2S81A has 12-bit resolution. All devices have user selectable dynamics. The AD2S80A is available in 40-pin DDIP, 44-pin LCC and is qualified to MIL-STD-883B Rev. C. The AD2S82A is available in a 44-pin PLCC, and the AD2S81A in a 28-pin DDIP.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Leaded Chip Carrier (P) Package



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